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APPLICATION NO. FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO. CONFIRMATION NO. 10/716,456 11/20/2003 Shigeo Kurakata XA-9984 6671 181 03/22/2006 EXAMINER 7590 MILES & STOCKBRIDGE PC CRIBBS, MALCOLM D 1751 PINNACLE DRIVE PAPER NUMBER ART UNIT **SUITE 500** MCLEAN, VA 22102-3833 2115

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applicat	ion No.	Applicant(s)
Office Action Summary		10/716,4	156	KURAKATA ET AL.
		Examine	er ·	Art Unit
		Malcolm	D. Cribbs	2115
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).				
Status				
2a) <u></u>	Responsive to communication(s) filed on <u>20 November 2003</u> . This action is FINAL . 2b) This action is non-final. Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.			
Disposition of Claims				
5)□ 6)፟⊠ 7)□	4) ☐ Claim(s) 1-10 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-10 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.			
Applicati	on Papers			
 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. 				
Priority under 35 U.S.C. § 119				
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 				
2) Notic 3) Inform	t (s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (F nation Disclosure Statement(s) (PTO-1449 or r No(s)/Mail Date <u>11/20/03</u> .		4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	

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DETAILED ACTION

Claims 1-10 are presented for examination.

Claim Rejections - 35 USC § 103

- 1. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toombs et al [US Patent No. 6,901,457] in view of Maul [US Patent No. 6,339,805].
- 2. As per claims 1, 6, 7, and 8, Toombs et al teach the invention, comprising: a plurality of external terminals [Col 2 lines 35-43]; an interface unit [Fig. 2 interface]; and an erasable and writable nonvolatile memory [Fig. 2 memory core].
- 3. Toombs et al do not teach the process of having a low resistance before the mode is determined and thereafter having a high resistance. Specifically, Toombs et al teach the method of determining a mode, based on an asserted level of a CS signal on the select line, after receiving an initialization signal (CMD); wherein the separate modes requires different operation conditions including voltage levels, resistances, and specific data in order to control and communicate with the card. However, Toombs et al fail to detail the level of the signal for resistance before determining the mode

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requested. A routineer in the art would have been motivated to look for a teaching for the possible level of the signal before the mode was determined.

- 4. Maul teaches another variable resistance method when a peripheral devise have been attached thereto. Maul teaches a method of selecting a low resistance when the assembly is plugged-in until it is determined and a time period has elapsed [Col 4 lines 24-48, and Col 4 lines 42-45]. In summary, Maul teaches a method of switching to a low resistance state to stabilize and smoothly couple to the power supply.
- 5. It would have been obvious to one of ordinary skill in the art to combine the teachings of Toombs et al and Maul, which are analogous art, because they both teach selecting a different resistance for an external device attached thereto. Maul covers the deficiency of Toombs et al by teaching the detail of selecting a low resistance when the device is first plugged-in.
- 6. As per claims 2-5, Toombs et al teach the claimed invention wherein the mode determination is in response to an initialization command [Fig 9 Col 4 lines 40-46], and setting a first or second mode based on select terminal being high or low respectively [Col 4 lines 32-61].
- 7. As per claims 9 and 10, it is obvious to one of ordinary skill in the art wherein the lowering/increasing of a resistor value is directly proportionate to lowering/increasing of

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impedance [Sakshaug et al [US Patent No. 4,335,417 Col 1 lines 16-23] and Jordan [US Patent No. 5,585,741 Col 17 lines 30-35] and Dayton [US Patent No. 5,095,282 Col 1 lines 43-48]; therefore when a low resistance value is selected the impedance is also lowered.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Malcolm D. Cribbs whose telephone number is 571-272-5689. The examiner can normally be reached on M-F 8AM-430PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Malcolm D Cribbs

Examiner

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March 14, 2006